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Open-source, multi-layer LSI design & fabrication framework for distributed IP development and education

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Abstract

Continuous development of Large Scale Integration (LSI) technologies based on Moore's law results in highly developed LSI technologies, as well as very high costs in design and fabrication and high design complexity. This fact prevents various users from contributing to the activities of designing LSIs, fabricating LSIs, and developing Intellectual Properties (IPs). On the other hand, the trend towards open-source has been attracting attention to overcome these problems and extend the potential of LSI technologies. The purpose of this research is to develop an open-source LSI design framework aimed at connecting various layers of LSI knowledge. Its methodology is composed of two parts. One is the development of the LSI design flow using existing open-source EDA tools and their related glue software. The other is the open-source, NDA-free PDK (process design kit) used in designing LSIs. The process of developing and constructing Large Scale Integrated (LSI) circuits within this framework is conducted and assessed. From these trials, the effect of enhancing educational effectiveness on LSI design is indicated. These trials enhanced the contributors' interest and motivation to understand the details of computer systems and their relation to LSIs. It is also indicated that this framework is effective in enhancing rapid IP development as well as its importance as an educational aspect of open-source software.

Keywords: EDA tools and PDK, IP development, LSI technologies, Moore's law, Open-source, Technology education.

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1. Introduction

The continuous development of LSI (Large Scale Integration or large-size integrated circuits (IC), which is also often called "semiconductor" or simply "chip") technologies based on Moore's law [1, 2] has facilitated the continuous progress of computers in terms of performance, size, and cost [2, 3]. It is also notable that this trend also realized the paradigm shift on the computer in applications, where the computer has become a component of the system, such as low-lost microcontrollers (MCU), resulting in user-friendly electronics, such as Arduino [4]. On the other hand, the highly developed LSI technologies also result in a drastic increase in the design and fabrication costs of LSI, such as the design complexity, the cost of design tools, and the fabrication cost. The increase in the cost of design and the initial cost of fabrication require a large mass of production for users to collect the initial cost. These phenomena have been forming barriers for newcomers in the education field and also for small startup companies as potential users of LSI technologies. In other words, they are also narrowing the deviation of LSI users and engineers, making the LSI technologies difficult to access for the users who really need them.

From the viewpoint of IP (Intellectual Property, or the designed circuit libraries) circulation in the market, although there are a lot of trials for analog IP circulation as well as digital IP, few have commercially succeeded. One of the factors that restricts circulating IPs is the NDA (Non-Disclosure Agreement) for designing and fabricating LSI between the fabrication company, such as TSMC, and the users in order to protect the technical knowledge of the fabrication companies. The lack of analog IP circulation is one of the severe problems facing the future analog LSI ecosystem, including EDA (Electronically Design Automation, which commonly means the design tool software) vendors, foundries, and the circuit & system designer.

On the other hand, the trend towards open-source has been attracting attention to overcome these problems and extend the potential of LSI technologies. For example, the open-source instruction set of microprocessors, RISC-V [5], has been attracting attention for the processors of embedded systems. Some projects are focusing on establishing the open-source ecosystem when designing LSI. For example, Google launched an open-source LSI design project in 2010 [3], especially focusing on the custom digital circuit design, including RISC-V (which is the processor's open-source instruction set).

The author has designed an open-source LSI design framework aiming at connecting various layers of LSI knowledge and the trials of designing and fabricating LSIs using this framework [6]. This framework is motivated by the technological and the educational trends of the Make: [7], the movement to bring the fabrication technologies back to the users who actually need them. This paper describes the details of this framework and discusses its effect on distributed IP development and the educational aspect.

2. History of LSI Technologies and their Impact on Electronics

2.1. Moore's Law and Its Effect

Moore's law is the prediction, or industrial trend, of LSI technology development proposed by Moore [1] based on the MOS transistor scaling effect proposed by Dennard [2], as shown in Figure 1. The effect of Moore's law is worth it for both the LSI fabricators and the LSI users in terms of performance, functionality, and cost [8] . It strongly leads the LSI technology's development to reduce the physical size of the transistors and the circuit. Recently, the big trend of AI and IoT applications required more and more transistors to realize smart and real-time processing systems, like the autonomous vehicle.

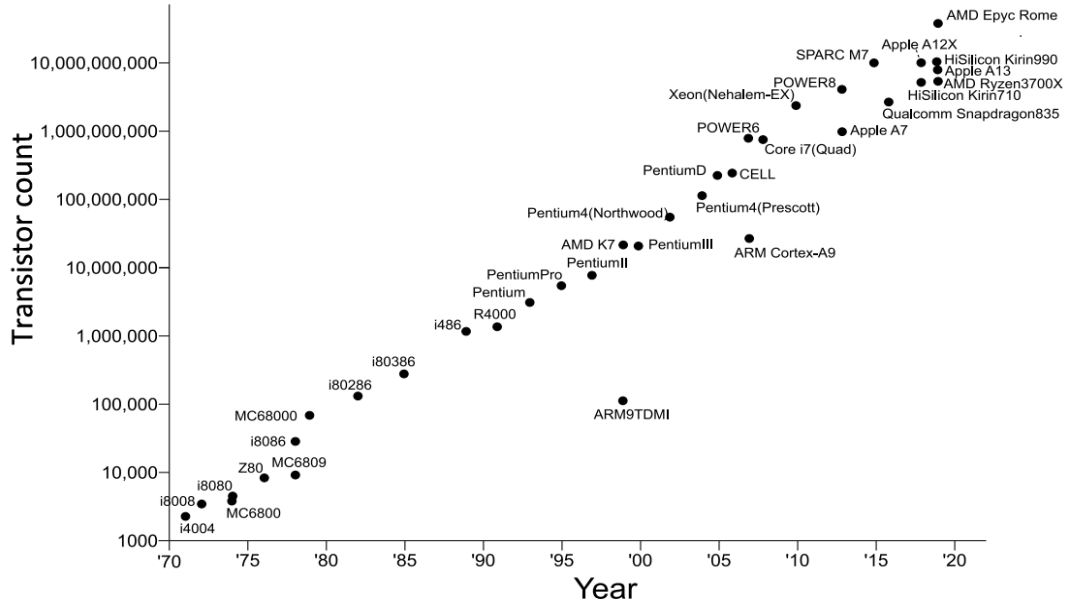

Figure 1.
Moore's law.
Source: https://ourworldindata.org/uploads/2020/11/Transistor-Count-over-time.png; Wikipedia (wikipedia.org/wiki/Transistor_count).

On the other hand, the cost of LSI design and manufacturing has significantly increased as a result of the reduction in physical circuit size and rise in circuit complexity. This particular feature presents a significant obstacle for anyone entering the field of LSI technology.

We can consider the effect of Moore's law on reducing the cost from other viewpoints than the simple reduction of computer system costs. The reduction of LSI costs also has the possibility of realizing a novel paradigm in LSI applications. For example, the single-chip micro controller (MCU) is a low-cost, small-sized computer with a classical architecture with embedded memory and peripheral subsystems that is fabricated using traditional technologies. We cannot only build simple devices, such as LED (Light Emitting Diode) blinking, using an MCU (Micro Controller Unit), but also consider the paradigm of using an MCU for LED blinking as the best solution from any viewpoint compared with other implementation technologies, such as a traditional RC oscillator. In other words, the cost reduction in LSI technologies has realized the paradigm shift in the computer and its related LSI application field, as shown in Figure 2.

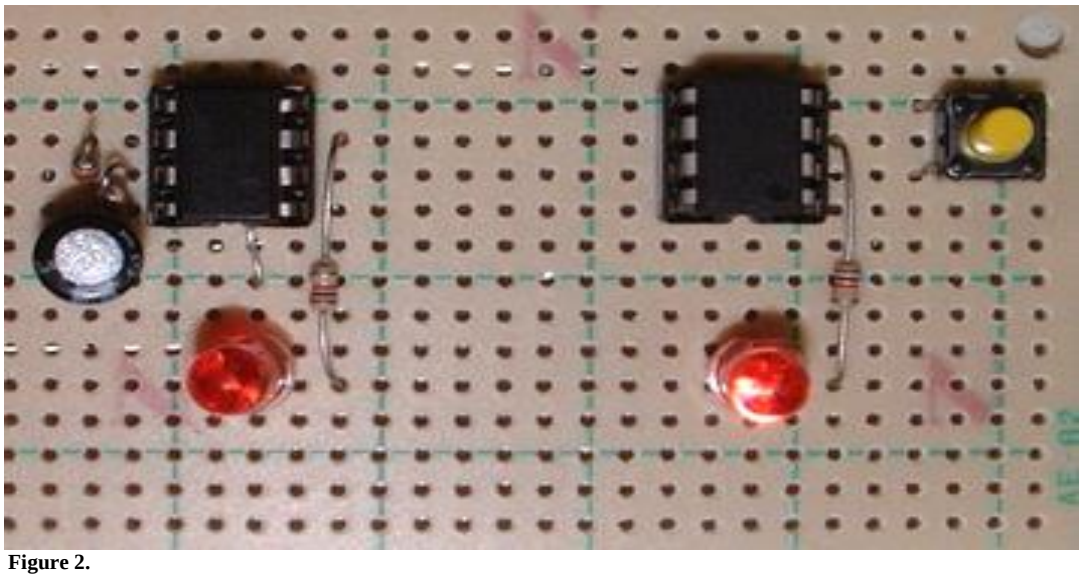

Figure 2.
Paradigm shift of LED blinking, (left) RC oscillator, (right) MCU. Now, (b) is not only possible, but also realistic.

In the area of IP circulation, there are a lot of trials for analog IP circulation as well as digital IP. For example, Design and Reuse is one of the companies that tried to commercially circulate analog and mixed-signal IPs, and Barcelona is one of the companies that tried to commercially realize the analog circuits synthesize. Although they are successful in a sense, few of them remain in commercial IP market. One of the reasons why the analog IP circulation commercially is limited is the complicated procedure for using it, or strict NDA between the fabrication company and the users. The NDA was originally intended to protect the knowledge and technologies of the fabrication companies while also restricting their ability to share the designed circuits in an open-source manner. Open-source is one of the important trends in software development [9] for enhancing the speed and quality of the developed software, as well as commercializing it and recruiting engineers. The lack of analog IP circulation is one of the severe problems facing the future analog LSI ecosystem, including EDA vendors, foundries, and the circuit & system designers.

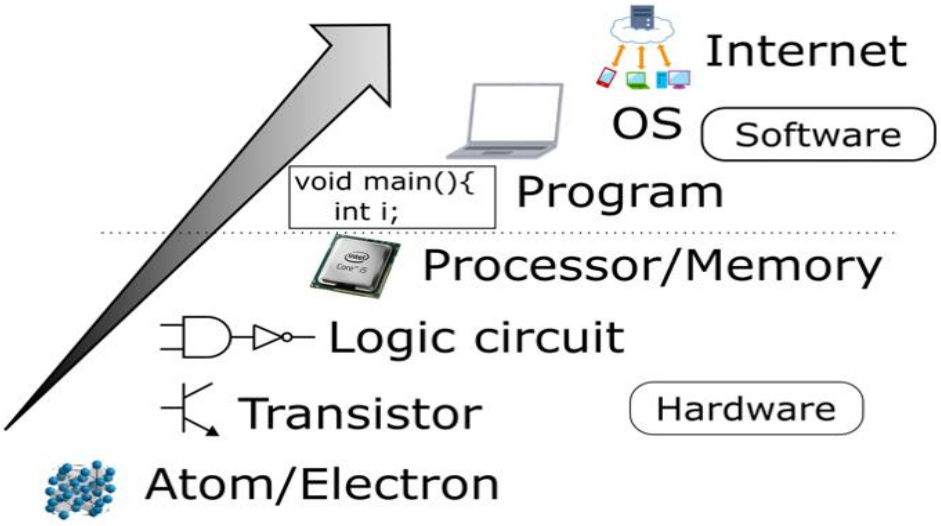

Figure 3.
Divided worlds of computer science.

From the viewpoint of education, the complex structure of the computers and LSIs makes the students understand the layers of technology. For example, the software field, such as developing software, compilers, and computer networks, is separated from the hardware field, such as circuit design and solid-state physics of semiconductors, as shown in Figure 3. This separation is realistic in terms of the restricted time of study in school; however, it often results in a "black box" problem. Although "black box" is efficient in understanding each field deeply and utilizing the technologies for applications, it often results in giving up understanding the contents of "black box", and prevents utilizing the potential of "black box". Actually, LSI is literally the "black box" for most of the engineers, except the LSI designers, and most of the users and engineers create ideas "by using" existing LSI components and never consider "what can be realized by using custom LSIs."

2.2. "Maker Movement"

In recent years, we have seen worldwide technical, educational, and social movements in the field of any kind of fabrication, including the electronics industries, called the "Maker Movement" [7]. We can summarize it as follows:

- The highly developed technologies enable the implementation of "additional functions", such as enhancing usability.
- The technology and its users who fabricate anything have been integrated, and this phenomenon results in bringing the fabrication technologies back to the users, or a kind of "democratization" of technologies. Not only the engineers, but all the users can utilize any kind of technology for their applications.
- This can realize the industry framework for filling the various demands of the users. Note that this framework is not a substitute for the traditional mass-production industries; they complement each other.
- The technologies of rapid prototyping, crowd funding, and the supply chain of components and their ecosystem have enabled many hardware start-up companies all over the world.

One of the important backgrounds of the "Maker Movement" is the fact that various fabrication technologies, such as circuit design, PCB fabrication, software development, and body design and fabrication, have been available for various users based on the highly developed digital technologies. This phenomenon is also called the democracy of technologies", which is also affecting the field of electronics. For example, only professional engineers and high-level amateurs have used electronic circuit design for building systems for a long time. However, electronics technologies have been extending their users to various kinds of people with various professions and interests, such as artists, designers, and hobbyists. They are exploring novel applications of the technologies that traditional engineers can't imagine. In other words, the wide variety of technology users is an important factor in creating innovations [9].

3. Related Works on Open-source LSI Design & Fabrication Framework

In this section, the author reviews related works on open-source LSI design frameworks and related technologies. In the big wave of the "Maker Movement", the LSI technology remains "un-democratized", for its high cost and highly developed complexity. LSI technology must be an implementation tool for everyone who needs it, and there are some projects aiming at "democratizing" the LSI technologies.

One of the most important trends to "democratize" LSI technologies is "open source" [10-12]. For example, Google has started an open-source LSI design project [3] with free-of-charge fabrication trials. It uses Sky Water's 130-nm fabrication facilities and provides the design kits using them. It has extended the choice of the fabrication process, such as Global Foundries' 90nm, and further. Their project is also developing a set of open-source EDA tools [13].

There are also some research projects on open-source EDA tools [14-17]. One category is the high-level EDA tools, which "compile" the circuit described by the language (HDL; hardware description language) into the silicon chip. There are some basic and fundamental open-source tools for logic synthesis [18] and place & route [19]. Their following projects are continuously developed and improved [20-22]. Although their performance may be less than that of commercial EDA tools, they achieve enough performance for a certain application. There are also studies on open-source FPGA tools [23].

For some building blocks of digital systems, there are also several projects, such as the open-source memory generator [24] and its application for the accelerator of neural network operations [25]. For the processor core, RISC-V is developed and widely used for implementing not only simple microcontrollers but also microprocessors that run Linux OS [26].

Circuit simulation is also an important piece of the LSI design flow. Berkeley's SPICE is one of the most famous and traditional open source circuit simulators, and its following projects are also continuously developed, integrating the digital circuit simulations [27]. The timing characterization of the digital circuit elements is required to establish high-level digital design flow, and there is some research to realize the open-source tools [28].

Parameter extraction tools are another category of EDA tools that extract simulation parameters from measured characteristics. There are also open-source EDA tools for parameter extraction [29].

The analog circuit was designed by mature designers for a long time, and there are research project to automate it, some of which are open source [30-32].

For low-level physical design tools, such as layout editors and layout verification, there are some open-source EDA tools, such as KLayout and MAGIC.

The design rules and simulation parameters are also important factors in establishing LSI design and fabrication. The chip fabrication companies, such as TSMC, provide this information for the LSI designers; however, they require an NDA (non-disclosure agreement) since this information contains a high-level secret on the fabrication facilities and business matters. The mature, old-fashioned fabrication process is also useful for many applications, and there are some approaches to realizing LSI design without an NDA [33-35]. MOSIS, a company providing LSI fabrication services in the US, released "scmos" (scalable CMOS (Complementary Metal-Oxide-Semiconductor, which is common device structure of recent LSIs)

[36] for starting LSI design. It is composed of the simplified LSI design rule based on classical Lamda-rule, the transistor simulation models, and the design configuration files for some commercial EDA tools. It supports several fabrication technologies available at MOSIS, with one physical size parameter called “lambda” to simplify the physical layout design of LSI. Chenouf, et al. [37] proposed the simplified 1um design rule, related PDK (Process Design Kit), and the design flow using the commercial EDA tools. It focuses the dedicated LSI fabrication facilities on the actual fabrication.

From the viewpoint of the educational aspects, there are some research projects on open-source, NDA-free LSI design courses [38-40]. Most of them use the low-level, physical design flow to provide the educational materials to help students understand the physical structure of the primitive function of LSI. The other approach is the high level, or top-down, design. For example, the focused users in Google’s project [3] are the designers of the embedded processors. The prepared frame for LSI design provides a RISC-V processor, and the user can design the original peripherals with it. Although the low-level design flow of drawing the physical layout of the transistors and the circuits by connecting the transistors is possible, the complicated design rule of layout prevents the user from smoothly understanding the relationship between the physical design and the circuit function. In other words, there remains the “black box” in LSI design, which prevents the user from understanding the whole flow of LSI design and fabrication. The level-crossing education material is important to make connections between low-level hardware and high-level functions of computers at the LSI design level.

4. Design and Trial of an Open-Source, Multi-layer LSI Design and Fabrication Framework

4.1. Motivation of an open-source, multi-layer LSI design and fabrication framework

As described above, the current LSI technologies are a "privilege" for those who can use them technically and financially and exist away from those who actually need them. For example, the armature hobbyist or the software engineer can’t imagine designing and fabricating the custom LSI, and they have to exclude the solution of using custom LSI for their purpose. This situation around the LSI technologies disables the majority of users (engineers, researchers, hobbyists, and so on) from thinking about the possibility of designing the custom LSI as an "implementation tool", Thus, they simply choose the existing technologies available in the commercial market, such as the computer system, electronic components, and so on.

For example, before the Microsoft Kinect appeared on the market, there were few research studies and projects using the depth camera in the user interface field. After the Kinect appeared on the market, numerous research projects using a depth camera for user interfaces appeared. This fact is considered to indicate that Kinect caused disruptive innovation in the user interface field. This fact indicates that the majority of users can use the available tools on the market for implementation. It is hard for most users to implement the tool itself as well as to think about the world in which the non-existing tools are available. Anyone can design and develop the Kinect if he or she can actually use the LSI technologies. It is important to think about the world with the possible tools, not the currently existing tools.

The situation of high cost and design complexity also causes the narrow variation of LSI technologies among engineers and users. Based on the experience of LSI design and the academic and industrial communities, the factors causing this situation are summarized into three factors as follows:

- Lack of a low-cost, easy-to-use design tool.
- Lack of low-cost, easy-to-use LSI fabrication methodologies.
- Lack of user community.

For the design tool, the current commercial LSI design tool is too expensive and too complicated, even for simple or personal-purpose LSI design for non-mass production usage. Some open-source EDA tools are available and being rapidly developed. While the functions of these tools are less than those of commercial ones, most of them have sufficient performance for certain applications. Since most of them are independent and separate tools, we have to combine them to establish the design flow.

For the fabrication methodologies, the current commercial LSI fabrication service is not only too expensive for personal or small business purposes, but the strict NDA also prevents users from spreading, sharing, and circulating the knowledge and designed circuits, or circuit IPs.

Users who deal with LSI technologies also experience the narrow variation as a result of these circumstances. For example, the specialists in LSI technologies have rich knowledge and experience in designing and implementing LSI systems. However, they have few experiences developing novel LSI applications from the viewpoint of wide application fields, such as AI, big data, IoT, social robotics, user interfaces, and so on. In the field of education, LSI technologies are too expensive and require a long time to fabricate for most students to start learning. The complicated process of designing LSI also takes the student a long time to reach the starting point of LSI design. The lack of design, fabrication, and evaluation experiments for students restricts their knowledge and experiments with LSI technologies.

4.2. Design of an Open-Source, Multi-Layer LSI Design and Fabrication Framework

In order to solve these situations, the author has designed an open-source, multi-layer LSI design and fabrication framework named [41]. It is composed of the following components:

(a) NDA-free design rule and PDK.
(b) Documents for integrating the existing open-source EDA tools and “glue” software to smoothly connect each tool’s outputs to form the design flow, as well as tutorial documents.
(c) LSI fabrication trials.
(d) Repository for sharing the designed circuits (IPs) and measurement results.
(e) On-line community for sharing experience and knowledge.

The design of this framework focuses on the low-level LSI design, where the users directly draw the mask data for LSI fabrication, along with circuit verification, as shown in Figure 4. The reason for skipping the high-level design is to solve the "black box" problem. In low-level LSI design, the user can understand the relationship between the physical layout, the circuit configuration, and the function of the circuit. It is also effective for educational purposes.

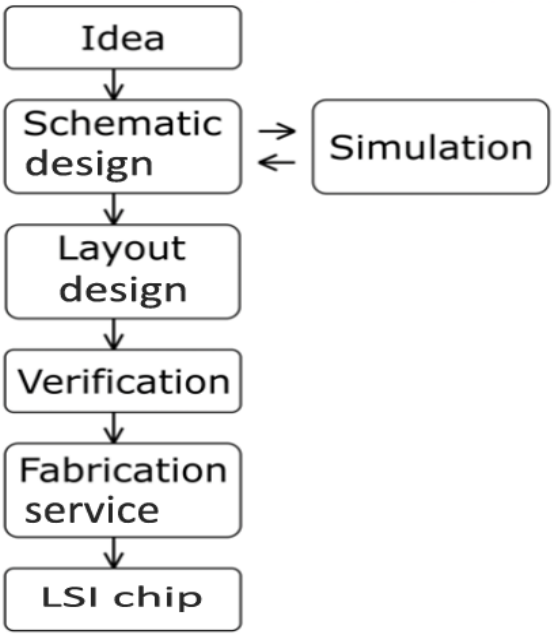

Figure 4.
Basic design flow.

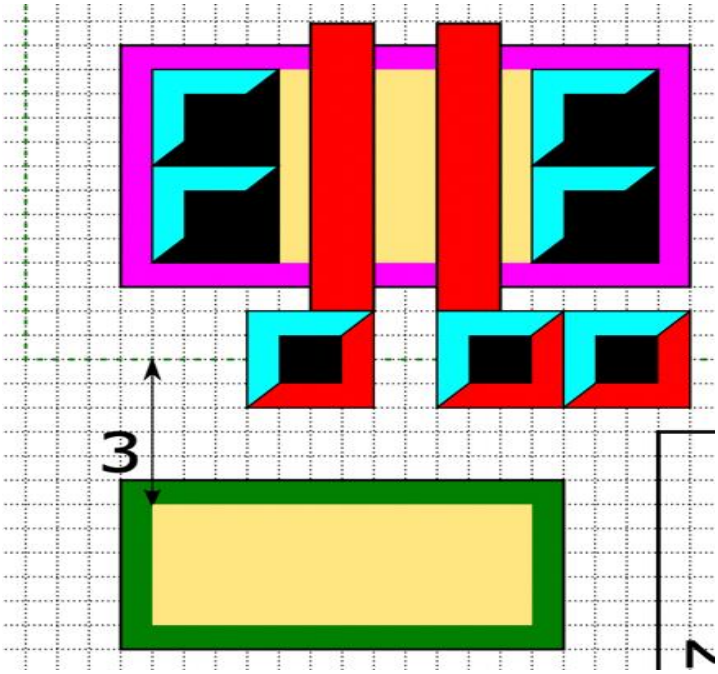

Figure 5.
Example of "1um-grid" rule and the original rule.

(a) is the basis of the project to design and fabricate the actual LSI chip. First, a fabrication company is selected that has agreed to disclose the design rules and PDKs. While the detailed design rule and PDK are under NDA, the "1um-grid" design rule is defined [41]. The design rule parameters are defined so that the physical size of the design under this rule will automatically satisfy the original design rule under NDA. This mechanism is enabled since most of the design rules defin the "minimum" size of the shapes in the layout, as shown in Figure 5. The grid of 1um has the advantage that users can easily understand and draw the layout of LSIs.

(b) is the tool for designing LSI. First, the open-source EDA tools are investigated for each step of LSI design, and the target tools are selected, whose details are described in Make LSI [41]. For physical layout design, including layout verification and schematic entry, K-Layout and EEscheme are selected. Some software scripts are developed to connect

them. For the circuit simulation, LTspice is selected, although it is freeware but not open-source, and the author will continue to investigate suitable open-source tools.

For (c), the contributors choose the LSI fabrication company that offers CMOS 0.6um, 3 metal layer technology at a reasonable price.

For (d), a public GitHub repository is used. Since all the information used to design the LSI in (a) and (b) is not under NDA, it is shared as open-source.

For (e), we prepared a mailing list and Discord to form a community of the contributors, where their knowledge and experience of designing, fabricating, and measuring LSIs, as well as their motivation, are shared and discussed. There are no requirements to join this community, and the wide variety of contributors, such as armature hobbyists, soft engineers, and LSI design engineers, is guaranteed. Currently, 317 people are in this community.

4.3. LSI Design and Fabrication Trails

The first LSI design and fabrication trial in the MakeLSI project was carried out in August 2015. The participants in this trial are called in this project, and 8 members finished designing 11 circuit layouts as follows, as shown in Figure 6.

- 4bit Kilburn adder.
- Guitar distortion effector.
- 1bit CPU (Central Processing Unit) (simple data path).
- 4-16 decoder.
- Ring VCO for audio FM modulation.
- LC-VCO.
- Band gap reference (BGR).
- Saw-wave oscillator.
- Operational amplifier.
- MOS transistor TEGs (Test Element Group).
- "555"-compatible timer.

These circuits were assigned to two 3.2x3.2 [mm] chips, as shown in Figure 7, and their physical layout data is stored and shared on GitHub. Contributed members performed the evaluation of the fabricated circuits. Some of the designed circuits operated as expected, while others didn't. The reason for the unexpected operation is mainly a mismatch in the transistor simulation model and a lack of design checks. Currently, 10 trials are finished, and all the design data and measurement data are shared as IPs. They vary from the MOSFET's (MOS Field Effect Transistor, which is a common transistor device used in recent LSIs) test, logic circuit from cell element to functional blocks, analog circuit, and mixed-signal circuit, such as a D/A converter.

5. Discussions

Trials of LSI design and fabrication by the contributors enabled the stockpile of IPs on GitHub. This indicates the possibility of a rapid user-contributing IP development scheme. The factors that enable this phenomenon are the following:

- The contributors use common design tools.
- The contributors share the process and their knowledge of design for design process improvements.
- The design rule without an NDA enabled sharing the design data as open source.
- The contributors had passion for designing the circuit they actually wanted to implement.

It was observed that there was knowledge exchange on starting LSI design, utilizing the EDA tools among the users. These are enabled by the common EDA tools, which are their "language." There is a wide variety of contributors, from beginners to professionals. The professionals lead the efforts to improve the design tutorial documents, circuit performance, and accumulation of the designed IPs. For the beginners, most of them have a passion for LSI design, but they have little knowledge, skill, or experience in LSI design. The professionals help them to smoothly start and develop the LSI design. The common "language" in the community is also helpful to enhance these kinds of communications among the contributors.

These factors are also used in open-source software [9] to accelerate the development and improvement of IPs. Although the user-contributing IP development scheme has a large advantage in terms of short development times, it has a disadvantage in terms of the possible low quality of developed IPs. A strategy to improve the IP quality through the evaluation of the circuit measurements is needed to guarantee the IP quality. This project indicated that the framework of open source is effective for not only software development but also SI design.

From the viewpoint of educational aspect, some college and university professors used LSI design trials as an educational purpose, the entrance training for LSI design researchers. It is also notable that some contributors joined the STEAM exhibition event to exhibit their own designed LSIs. These activities, using the originally designed LSIs and explaining their experiences with their own voice, are expected to bridge the gap between the LSI designer and the LSI users. Since the MakeLSI framework is designed to go from the physical layout to the circuit function over the layers, it is expected to be effective in the STEAM (Science, Technology, Engineering, Art, and Mathematics) educational aspects.

From the viewpoint of fabrication methodology, the fabrication company often changes the fabrication service's processes. For example, the CMOS 0.6um process that MakeLSI is using now might be obsolete due to business matters, the lifetime of fabrication equipment, and so on. It is desirable to fabricate one designed circuit on various fabrication

processes, which is called “process transfer”. The author has been starting the multi-process-transferable LSI design framework [42], which will be tested in future works.

6. Conclusions

This paper presents an overview of MakeLSI, a freely available framework for designing and fabricating multi-layer LSI (Large Scale Integration) circuits. The primary objective of MakeLSI is to promote diversity and variability among users of LSI technology. The realisation of the quick intellectual property (IP) development programme, which incorporates user contributions, is accomplished through the utilisation of an open-source framework that leverages readily accessible technology. Moreover, it is important to acknowledge that the inclusion of a wide array of authors guarantees a comprehensive exploration of the potential use of LSI, a technology renowned for its effectiveness in the field of education..

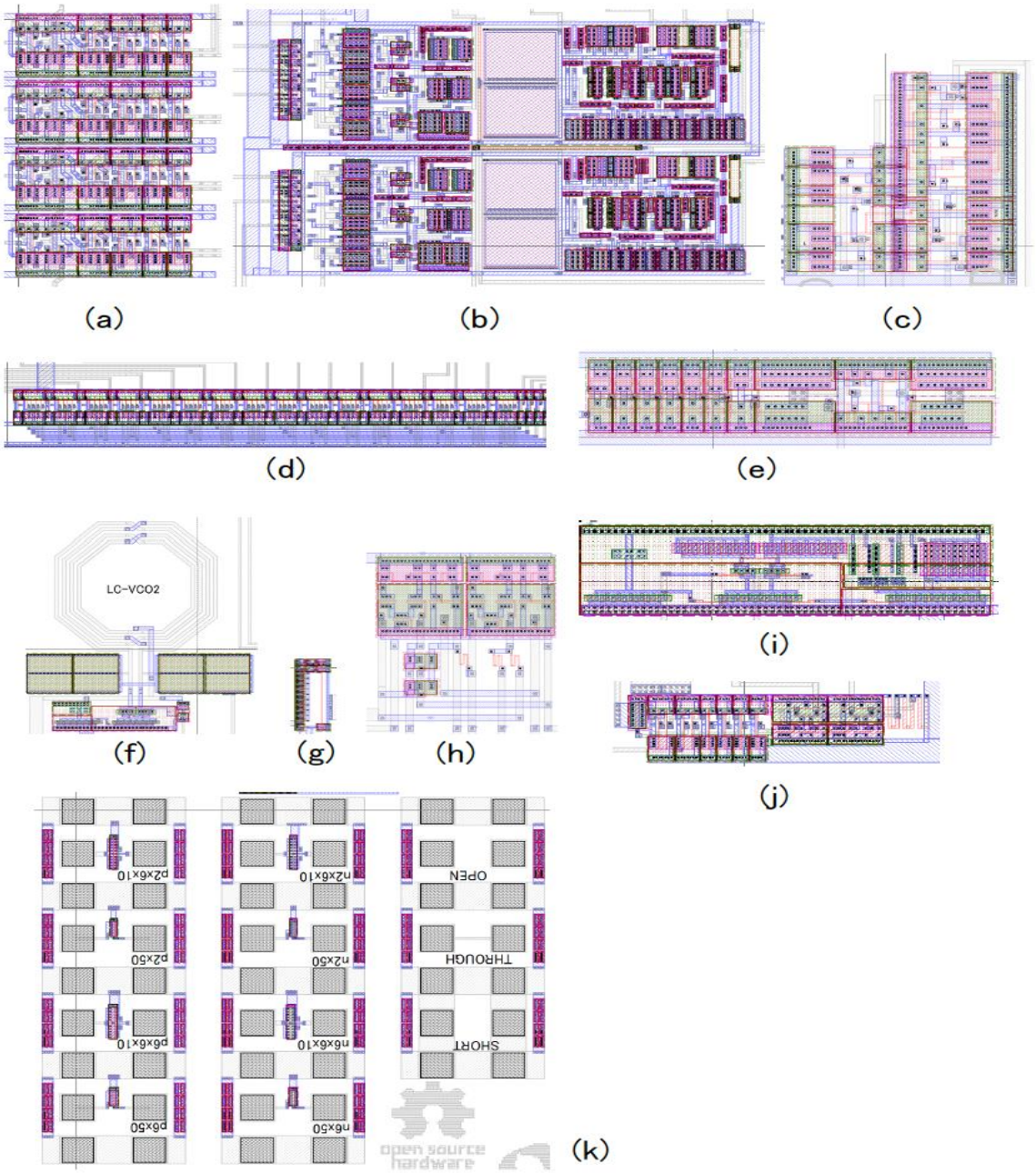

Figure 6.
Layout of designed circuit by contributors.

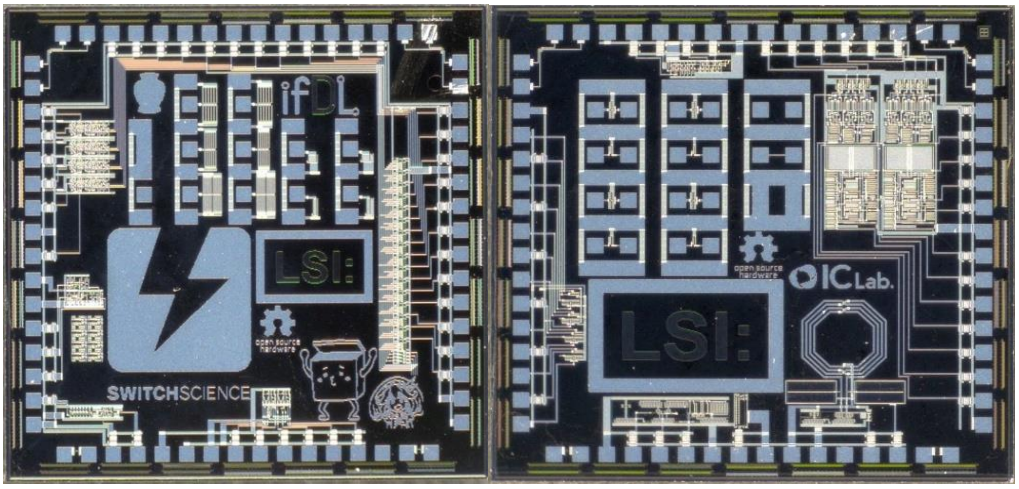

Figure 7.
Microphotograph of fabricated chips.

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